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Inventor(s): James John Casto, Qadeer Ahmad Qureshi, and Hugh William Boothby
Title: INTEGRATED CIRCUIT PACKAGE INCORPORATING PROGRAMMABLE ELEMENTS

Enclosed are:

19 Pages of Specification (including Written Description, Claims and Abstract)
8 Sheets of Drawings, ☒ Formal / ☐ Informal
☒ Declaration for Patent Application (4 pages), ☒ Executed / ☐ Unexecuted
☒ Assignment of the Invention (7 pages, including Cover Sheet)
☐ Information Disclosure Statement (_____ pages)
☐ with Form(s) PTO 1449 (_____ page(s)) and copies of _____ reference(s)
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CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Fee
Basic Fee =				690.00
Total Claims	38 - 20	= 18	x $18.00 =	324.00
Independent Claims	5 - 3	= 2	x $78.00 =	156.00
Multiple Dependent Claims (if any) - $260.00 fee				0.00
Other: N/A				0.00
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INTEGRATED CIRCUIT PACKAGE INCORPORATING PROGRAMMABLE ELEMENTS

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BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to integrated circuits and more particularly to integrated circuit packaging.

Description of the Related Art

Integrated circuits such as microprocessors can be run at different clock speeds and with different supply voltages. The determination of what is the appropriate clock speed and appropriate voltage depends on many factors. A higher clock speed requires a higher supply voltage. In addition, the higher clock speed results in additional heat and power being dissipated. Microprocessors utilized in mobile applications are particularly sensitive to power dissipation and generally require the lowest power dissipation and thus require the lowest supply voltage that can achieve the rated clock speed. Microprocessors used in desktop applications are less sensitive to power dissipation considerations.

In general, microprocessor product yield, performance (MHz) and reliability are affected by the voltage supply setting. Within a range of only several hundred millivolts, dramatic differences can be seen in yield, performance and reliability, even from the same wafer lot. Choosing the best voltage is usually a compromise of yield, performance and reliability since the same value of voltage is usually chosen for a large population.

A higher percentage of a given population of microprocessors could operate at higher performance levels (thus creating higher revenue) if each microprocessor could operate at its own specific voltage. One solution would be to mark each processor with a number or symbol indicating its voltage and/or speed rating. However, that provides no guarantee that the appropriate voltage is supplied to the microprocessor in the final system.

Referring to Fig. 1, one prior art approach for providing the appropriate voltage and frequency values in a computer system is illustrated. Central processing unit (CPU) 101 receives bus frequency signals 103 (BF[2:0]), which provide a multiplier used by the processor to multiply a bus clock (not shown). The multiplied bus clock is used by the CPU to clock its internal logic. CPU 101 also receives core voltage 105 (commonly referred to in x86 architectures as Vcc2) from CPU core voltage regulator 107. Other voltages, which are typically supplied to the CPU, e.g., Vcc3 (I/O voltage) are not shown. Core voltage regulator 107 is programmable and receives voltage control inputs 109 (also referred to as voltage ID (VID) signals) which determine the voltage level supplied to CPU 101. The values for the both the VID signals and the BF pins are provided by the settings of jumpers 111.

It is conceivable to set the jumpers to correspond to the marking (number or symbol) on the processor that indicates its voltage and/or speed rating. However, that approach provides no guarantee that appropriate voltage and frequency settings will be utilized. In fact, certain unscrupulous suppliers of computer systems have been known to provide systems having higher than recommended voltages and frequencies. Since companies typically qualify chips at certain voltage and frequencies, such over clocking or excessive voltage can result in shorter product lifetimes, decreased reliability and excessive product returns.

Providing information to users, which specifies the correct voltage and hoping that the correct voltage is subsequently supplied to the processor by circuitry on the board, is subject both to intentional misuse and unintentional error. In addition, the more possible voltage settings that are provided, the greater the possibility for error.

An additional factor to be considered is that if information on the preferred operating voltage and frequency for a specific chip is available only after testing that

chip, programming that information on the die after testing requires that additional processing steps be performed on the die. Those additional processing steps may cause increased cost.

Thus, it would be desirable to be able to specify the correct voltage for a processor and to minimize the opportunity for deliberate over clocking or over voltage and to minimize the possibility of error. Further, it would be desirable to obtain higher aggregate performance from a given population of microprocessors by specifying the proper voltage that individual processors should receive without unduly complicating the manufacturing process.

SUMMARY OF THE INVENTION

Accordingly, the invention provides in one embodiment, a package for mounting at least one integrated circuit die. The package includes at least one one-time programmable element, such as a fuse, having a first and a second end separated by a programmable link. The first end of the one-time programmable element is coupled to a power supply voltage node in the package. The second end of the programmable element may be coupled to an external package connection (e.g., a package pin) and/or to an internal package node that connects to an input terminal of the integrated circuit die when the integrated circuit die is mounted.

In another embodiment, a package for mounting at least one integrated circuit die includes at least one programmable element pair having a first and second programmable element. One end of each programmable element is coupled together through an internal package node. A second end of the first programmable element is coupled to a first internal power supply node and a second end of the second programmable element is coupled to a second internal power supply node. The internal package node may be coupled to an external package connection (e.g., a package pin) and/or to another internal package node that connects to an input terminal of the integrated circuit die when the integrated circuit die is mounted.

In still another embodiment, an electronic device includes a package having one or more programmable elements. The first end of one programmable element is coupled to a power supply node in the package. At least one integrated circuit die is

mounted in the package. The second end of the programmable element may couple to an external package connection (e.g. a package pin) and/or to an internal package node that connects to an input terminal of the integrated circuit die.

Still another embodiment provides a method for setting a parameter value for an integrated circuit. The method includes selectively programming one or more programmable elements located on an integrated circuit package, to selectively couple an internal package node a supply voltage node. The one or more programmable elements are selectively programmed according to a desired value of an integrated circuit parameter. The parameter may, e.g., be a voltage or speed rating. The internal package node is coupled to either a package pin, an input terminal of the integrated circuit or both.

In still another embodiment a method is provided that includes selectively programming at least one fuse of a fuse pair located on an integrated circuit package to selectively couple an internal node to either a first power supply voltage or a second power supply voltage. The internal node is coupled to a package pin or to an input terminal of the integrated circuit die mounted in the integrated circuit package, or to both.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

Fig. 1 shows a prior art approach to providing voltage and frequency settings.

Fig. 2 illustrates a high level system view of one embodiment of the present invention.

Figs. 3A-3C illustrate various fuse configurations.

Figs. 4A-4B show different views of another fuse configuration.

Fig. 5 shows a schematic of one of the fuses in Figs. 4A or 4B.

Figs. 6 shows another fuse configuration for providing information to package terminals.

Figs. 7 shows another fuse configuration for providing information to input terminals of the integrated circuit die.

Fig. 8 shows an embodiment in which fuses are placed in series with the package I/O terminals.

Fig. 9 shows an embodiment in which the various embodiments shown in Figs. 6-8 are combined.

Fig. 10 shows a schematic of the fuses shown in Figs. 6 -8.

Fig. 11 shows another embodiment in which a fuse provides ECC information to a processor.

Fig. 12 shows one embodiment of an antifuse structure.

Fig. 13 shows an antifuse in parallel with a fuse.

The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

Referring to Fig. 2, an overview of a system incorporating one embodiment of the present invention is illustrated. Fig. 2 show microprocessor 201 which includes package 203 that holds integrated circuit die (also commonly referred to as chip) 205. Package 203 includes fuses 207. Based on the programming of fuses 207, the package supplies voltage regulator 209 with VID signals 211. Based on the VID signals, voltage regulator 209 supplies core voltage 212 to processor 201. In addition, the package may supply system controller 213 (e.g. a north bridge including a memory controller and a PCI bridge) with frequency ID signals 215 which indicate the system clock multiplier at which the processor core operates. The fuses may also supply one or more parameters to chip 205.

Package 203 includes a number of external connections such as those providing VID signals 211. Note that the term package as used herein is intended to include any integrated circuit carrier. The exact nature of the external connection between the package and the card to which it attaches, e.g., a motherboard or daughter card, varies according to the type of package. For example, connection between the package and the board may be through package pins such with Pin Grid Array (PGA) packages, or using other interconnection technologies such as tape automated bonding (TAB), chip scale package (CSP) technologies, or ball grid array (BGA) packages.

In addition to the external connections, the package provides connections between chip 205 and package 207. The connection between chip and package varies according to the type of package. Typical package/chip interconnection technologies include wirebonding, flip chip connections and tape automated bonding (TAB). The connections between the package and the chip and the package and the board provide for signal input/output (I/O), which convey signal information to and from the integrated circuit chip. In addition to signal I/O, the package connections provide connections for Vss and Vcc.

A wide variety of package technologies exist that can exploit the present invention. The packages are typically multi-layered packages with vias providing interconnections between the various layers. For example, package 203 may be a multi-layer fiberglass laminate made of FR4 or FR5 fiberglass, Bismaleimide Triazine (BT) Resin, or other types of organic laminate structures known in the art. The packages described herein are exemplary only and any ceramic or organic package or other package formed of other suitable material that can accommodate programmable interconnections such as fuses may used in practicing the invention.

As shown in Fig. 2, fuses specifying operating parameters such as voltage may be formed on the surface of the package. The fuses may be formed by a metalization pattern on the package surface that connect through vias to other layers of the multi-layer package and subsequently to interconnections between the chip and package, external package connections, or both. The metalization patterns may be screen printed metalization patterns.

A laser process (e.g., using a CO2, UV or a diode pumped Nd:YAG laser) may be used to program the fuses by ablating away a portion of the metalization pattern once the appropriate setting(s) for the fuse or array of fuses are known. The amount of the fuse that is ablated away may vary. For instance, the programming of the fuse may only require a cut sufficient to provide an open circuit. Alternatively, substantially all of the conductive material residing on the surface of the package may be ablated away to minimize the risk of accidental (or intentional) shorting of the fuse afterwards. By programming an array of fuses, the appropriate "data" for operating the processor (e.g., voltage or frequency control values) may be specified. The fuse area on the package can then be covered with a suitable insulating material such as epoxy or silicone to prevent later tampering or accidental damage.

Figs. 3A - 3C illustrate various programming possibilities for exemplary fuses. The fuses are formed by metal traces, or other suitable conductors, which connect to vias, indicated by dark circles at each end of the fuse. The vias shown, in general connect to package pins (i.e. external package connections), package power supply nodes (Vss or Vcc) or internal package nodes that connect to the integrated circuit die when it is mounted on the package. The particular connection depends on the type of information intended to be specified by the fuses. Figure 3A shows the fuses prior to programming.

The fuses shown in Fig. 3A determine four bits of information. Each bit requires at least one cut. As shown in Fig. 3A, the top row of fuses 301-304 couple through vias 306-309 to Vcc. The top row of fuses also connect to vias 310-313, which in turn are coupled to package pins to provide four VID bits for connection to a voltage regulator. The bottom row of fuses 315-318 couple at one end through vias 320-323 to Vss. At the other end, the fuses couple to vias 310-313 and thus connect to one end to the top row of fuses 301-304.

Each of the fuses 301-304 and 315-318 include a fusible link coupling each end of the fuse formed by the metal trace or other suitable conductor. Referring to Fig. 3B, the programming shown provides a binary setting of 1-0-0-1 as the value of the fuses, where 1 is Vcc and 0 is Vss. That is, fuses 315 and 317 are blown causing

vias 310 and 312 to be coupled only to Vcc. Fuses 302 and 304 are also blown causing vias 311 and 313 to be only coupled to Vss.

If the circuit that receives the value programmed by the fuses can differentiate an open circuit from both a high and low voltage, i.e., if the receiving circuit can utilize ternary logic, then additional voltage settings can be provided using fewer pins. For example, referring to Fig. 3C, three VID pins provide 27 separate options. Fig. 3C shows a fuse programming of 1-0-2 where 2 is Vcc, 1 is floating and 0 is Vss. That is, the fuses are blown at 324 and 326 to provide a float at node 329. Additionally, the fuses are blown at 328 and 330 to provide a 0 and 2 respectively on nodes 331 and 333.

In addition to the four package pins required in Figs. 3A and 3B and the three package pins required in Fig. 3C, an additional package pin may be required in order to provide a special Vcc pin for testing purposes. Otherwise, the package may have its Vcc and Vss planes shorted together during package and integrated circuit testing prior to programming of the fuses.

Note that the use of the term "package pin" is used herein for convenience in describing certain embodiments. While the term is used herein to sometimes describe pins of PGA packages, the term is also used generally herein and is intended to encompass any external connection or contact between the package and the board.

Rather than provide fuse pairs to determine each VID value as illustrated in Figs. 3A-3C, alternatively a single fuse can be used to selectively couple a package pin to a power supply voltage. For example, referring to Fig. 4A, the values for VID are provided by fuses 401-404. Each bit requires at most one cut. Fuses 401-404 couple through vias 406-409 to external package connections and provide, e.g., four VID bits for connection to a voltage regulator. The fuses also connect to vias 410-413, which in turn are coupled to Vss.

If fuse 401 is blown, then the package pin is not connected to Vss. An external pull-up circuit is required to set the package pin to Vcc (unless the receiving circuit can distinguish a float from a ground). Fig. 4B shows another representation of the fuses shown in Fig. 4A. Each of the fuses shown in Figs. 4A and 4B is

represented by the circuit shown in Fig. 5, which shows fuse 501 coupled to Vss through a low resistance resistor 502 (0 ohms is acceptable) and to package pin 503. The configuration shown in Fig. 4 requires a maximum of only one cut per bit of information but does require external pull-up circuits. The minimum number of cuts for four bits of information is 0 while the maximum number of cuts is four. With the four fuses shown in Figs. 3A or 4A, up to sixteen different voltage ID values may be specified. Cut here refers to blowing the fuse, typically using a laser, although other method are possible as described further herein.

While the power supply voltage on the package shown in the embodiment in Figs. 4A and 4B is Vss, it is of course possible to instead provide a one-time programmable connection to Vcc on the package and have an external pull down circuit.

Other parameters may also be specified rather than voltage. For example, as described with relation to Fig. 2, frequency ID information may also be specified.

Referring to Fig. 6, another fuse configuration is illustrated which provides four bits of information. The fuses are again configured in pairs (e.g., fuses 601 and 602) in a manner similar to Figs. 3A-3C. The top fuses 601, 603, 605 and 607 of each pair couple to Vcc through resistors in resistor pack 610. The bottom fuse of each fuse pair, fuses 602, 604, 606 and 608, couple to Vss through resistors in resistor pack 612. The resistors provide a voltage divider function and thus, an extra test pin (to avoid having Vss shorted to Vcc during testing prior to programming of the fuses) may not be necessary. In the embodiment shown in Fig. 6, each of the fuse pairs couple respectively to common nodes 614-617. The common nodes 614-617 couple to external package connections, e.g., package pins. In other embodiments, the common nodes may couple only to external package connections (package pins) or only to the chip and not utilize package pins.

Fig. 7 illustrates an embodiment in which the value specified by the fuse array is provided to the integrated circuit instead of going to the package pins. Internal nodes 614-617 couple to, e.g., C4 pads coupling the die to the package. The fuse

array may be specifying a voltage, frequency or other parameter to the integrated circuit die.

Fig. 8 illustrates an embodiment in which fuse elements 624-627 are coupled serially between common nodes 614-617 and external package pins 620-623. The fuses 624-627 can be used in testing environments, where for example, an internal signal must be accessible during test but is then decoupled from the package pin by blowing the fuse prior to product shipment. Fig. 9 illustrates an embodiment combining the various embodiments illustrated in Figs. 6-8. A schematic of one of the fuse pairs in Fig. 6-9 is shown in Fig. 10.

In order to program the fuse configuration shown in Figs. 6-10, at least one fuse of each pair must be blown to connect the common node to either Vcc or Vss. Thus, for four bits of information, four cuts are generally required. If three state logic is available then both fuses of a pair can be cut to represent a third value.

Referring to Fig. 11 another embodiment illustrates a fuse, without the voltage divider configuration used in Figs. 6-10, providing a parameter value to the integrated circuit die mounted on the package. In the particular embodiment, a signal is provided to that selectively enables error correcting code (ECC) according to the state of the fuse. The ECC signal may be used, e.g., for an on-board cache for a microprocessor. An internal pull-up is required in the processor to specify a value if the fuse is not cut.

The description so far has described cutting fuses with lasers. Several alternative embodiments are also possible. For instance, while the fuses have been described as being laser programmable, the fusible links may also be programmed electrically in a manner known in the art. That is the fuses may be fabricated as electrically programmable fuses. Further, while the fuses have been described as being on the surface of the package, the fuses may actually be fabricated on internal layers of a multi-layer package and be fabricated out of a conductive material other than metal. If fuses are on a layer other than the surface of the package, then electrically programmable fuses may be preferred.

Further, while the embodiments so far have been described using fuses to provide one-time programmable interconnections to supply voltages and to external and internal package connections, antifuses may also be used. A fuse provides a normally short circuit that turns into an open circuit when fused, using either electrical or laser programming. An antifuse is another type of one-time programmable interconnect that is equally applicable in the context of the present invention. An antifuse provides a normally open circuit that is short circuited when fused. Thus, both the fuse and antifuse are structures having two ends connected by a programmable link that, on application of suitable laser or electrical programming results in either an open or short circuit, respectively.

Wherever embodiments have been described herein as using fuses, such as in Figs. 2-11, other embodiments utilizing antifuses are also contemplated. In that case, programming is typically opposite of the fuse embodiments as is readily apparent to those of skill in the art. One advantage of using antifuses in the context of the present invention is that the extra Vcc pin that may be required in, e.g., Figs. 3A-3C to avoid Vcc being shorted to Vss during test, may be eliminated.

In one embodiment, an antifuse such as the one illustrated in Fig. 12 may be utilized. The antifuse 120 includes a generally circular conductive area 121 which is in electrical contact with via 122. Via 122 may couple, e.g., to a power supply node. Via 123 is not in electrical contact with via 123. If it is desired to short via 122 and 123 together, then conductive paste or solder may be deposited so as to form an electrical contact between via 123 and via 122 and circular conductive area 121. The conductive paste may then be subject to ultraviolet curing.

In another embodiment, an antifuse is combined in parallel with a fuse to provide the capability of reversing a fuse cut. Referring to Fig. 13, antifuse 130 including circular conductive area 131 in electrical contact with via 132. In this embodiment, via 132 is electrically connected to via 133 via fuse 134. If fuse 134 is blown, that can be reversed at a later time by programming antifuse 130, i.e. shorting vias 133 and 132 using solder as described above. Other antifuse approaches may also be used.

While the embodiments have generally been described with relation to a package containing a single integrated circuit and particularly a microprocessor, multi-chip modules may advantageously exploit one or more of the various embodiments described herein. In addition, the invention is not restricted to microprocessors. Other types of integrated circuits may also utilize one or more of the various embodiments described herein.

One advantage of the present invention is the that testing procedures to characterize the part may be completed prior to programming of the fuses. Thus, the part in question may complete tests on automatic test equipment (ATE) as well as system level tests. Once the tests are completed and the part is characterized in terms of voltage and speed, the package may be programmed without having to perform any further processing steps on the die or any further testing, except to check that the fuses were appropriately programmed. Of course, the fuses may be programmed prior to mounting the die if the values for the fuses are known.

Because each part may have its optimum voltage and/or other parameters specified, voltage parameters may be specified with more granularity. Thus, higher aggregate performance from a given population of microprocessors may be achieved by specifying the proper voltage that individual processors should receive. That is, the same value for voltage no longer has to be chosen for as large a population of microprocessors. Of course, the system in which the packaged part is utilized must be able to exploit any signals specified by the fuses and provided to the system.

The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. Variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A package for mounting at least one integrated circuit die, the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package.

2. The package as recited in claim 1 wherein the programmable element is one of a fuse and an antifuse.

3. The package as recited in claim 2 wherein the package is a multilayered package and the programmable element is formed of a metalization pattern located on a surface of the package.

4. The package as recited in claim 2 wherein the package is a multi-layered package and the programmable element is located on a layer other than the surface of the package.

5. The package as recited in claim 2 wherein the programmable element is covered by a protective layer.

6. The package as recited in claim 2 wherein the programmable element is not covered by a protective layer.

7. The package as recited in claim 2 wherein the second end of the programmable element is coupled to at least one of an external package connection and a package contact that connects to an input terminal of the integrated circuit die, after mounting of the integrated circuit die.

8. The package as recited in claim 2 wherein the programmable element is coupled to the power supply terminal through a resistive element.

9. The package as recited in claim 2 wherein the second end of the programmable element is coupled to an external package connection and to an

internal package node that couples to an input terminal of the integrated circuit die when the integrated circuit die is mounted.

10. The package as recited in claim 2 wherein the programmable element is programmable using a laser.

11. The package as recited in claim 2 wherein the programmable element is programmable using an electrical current.

12. The package as recited in claim 2 further comprising another programmable element coupled between the second end of the programmable element and an external package connection.

13. The package as recited in claim 1 further comprising a second one-time programmable element coupled in parallel with the one time programmable element and wherein the one one-time programmable element is a fuse and the second one-time programmable element is an antifuse.

14. The package as recited in claim 2 wherein the package includes at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element.

15. The package as recited in claim 14 wherein the internal package node is coupled to at least one of an external package connection and an input terminal of the integrated circuit die, after mounting of the integrated circuit die.

16. The package as recited in claim 14 further comprising a first resistive element coupled between the internal package node and the power supply node and a

second resistive element coupled between the internal package node and the second power supply node.

17. An electronic device comprising:

a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node; and

at least one integrated circuit die mounted in the package.

18. The electronic device as recited in claim 17 wherein the one or more programmable elements specify one or more operating parameters relating to the electronic device.

19. The electronic device as recited in claim 18 wherein the integrated circuit die includes a processor and the one or more operating parameters specify an operating voltage of at least a portion of the processor.

20. The electronic device as recited in claim 17 wherein the internal package node is coupled to at least one of an external package connection and the integrated circuit die.

21. The electronic device as recited in claim 20 wherein the internal package node couples to an external package connection through another programmable element.

22. The electronic device as recited in claim 17 wherein the package is a multilayered package and the programmable element is located on a surface of the package.

23. The electronic device as recited in claim 17 wherein the package is a multi-layered package and the programmable element is located on a layer other than the surface of the package.

24. The electronic device as recited in claim 17 wherein the one or more programmable elements, when programmed, specify a control value relating to clock frequency at which the processor operates.

25. The electronic device as recited in claim 17 wherein a state of the programmable element specifies use of error correction code (ECC) for a cache memory on the processor.

26. The electronic device as recited in claim 17 wherein the one one-time programmable element is part of a one-time programmable element pair, the programmable element pair including a second one-time programmable element in addition to the one one-time programmable element, the second programmable element having a first end coupled to the internal package node and a second end coupled to a second power supply voltage.

27. The electronic device as recited in claim 26 further comprising a first resistive element coupled respectively between the internal package node and the first power supply node and a second resistive element coupled between the internal package node and the second power supply node, thereby providing a voltage divider when the first power supply node is electrically coupled to the second power supply node through the programmable element pair.

28. A method for setting a parameter value for an integrated circuit, comprising:

selectively programming one or more one-time programmable elements located on an integrated circuit package, thereby selectively coupling an internal package node to a supply voltage node.

29. The method as recited in claim 28 wherein the one-time programmable elements are one of a fuse and an antifuse.

30. The method as recited in claim 29 wherein the internal package node couples to at least one of an external package connection and an input contact of an integrated circuit die.

31. The method as recited in claim 29 wherein the specifies an operating voltage for at least a portion of the integrated circuit.

32. The method as recited in claim 29 wherein an integrated circuit die is mounted on the package when the one or more one-time programmable elements are being selectively programmed.

33. A method comprising:

selectively programming a first programmable element of a programmable element pair located on an integrated circuit package to selectively couple an internal node to a first power supply voltage; and

selectively programming a second programmable element of the programmable element pair to selectively couple the internal node to a second power supply voltage.

34. The method as recited in claim 33 wherein the internal node is coupled to at least one of an external package connection and an input terminal of an integrated circuit die mounted in the integrated circuit package.

35. The method as recited in claim 33 wherein the first power supply voltage is ground (Vss).

36. The method as recited in claim 33 wherein the second power supply voltage is Vcc.

37. An apparatus comprising:

a semiconductor package; and

means for specifying a parameter value for the apparatus.

38. The apparatus as recited in claim 37 further comprising a processor mounted in the semiconductor package.

INTEGRATED CIRCUIT PACKAGE INCORPORATING PROGRAMMABLE ELEMENTS

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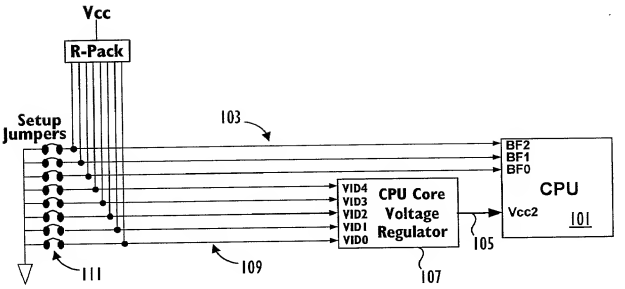
Hugh William Boothby

ABSTRACT OF THE DISCLOSURE

An integrated circuit package includes at least one one-time programmable element, such as a fuse, having a first and a second end separated by a programmable link. The first end of the one-time programmable element is coupled to a power supply voltage node in the package. The second end of the programmable element may be coupled to an external package connection (e.g., a package pin) and/or to an internal package node that connects to an input terminal of the integrated circuit die when the integrated circuit die is mounted in the package. The information programmed by the fuses may relate to speed or voltage ratings for a microprocessor.


Vcc
R-Pack
Setup
Jumpers
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BF2
BF1
BF0
CPU
Vcc2
101
VID4
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VID0
CPU Core
Voltage
Regulator
105
107
109
111

Fig. 1

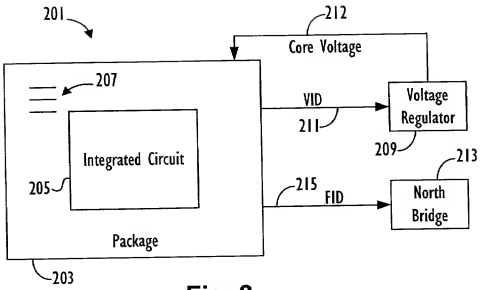

Fig. 2

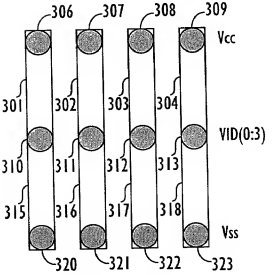

Fig. 3A

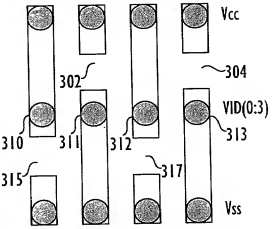

Fig. 3B

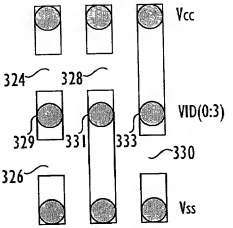

Fig. 3C

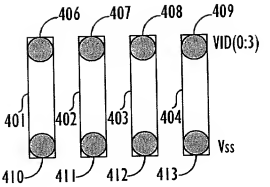

Fig. 4A

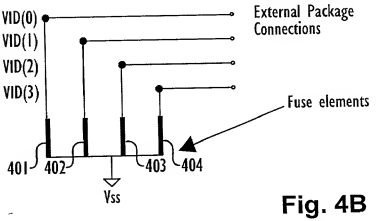

Fig. 4B

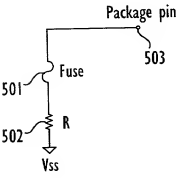

Fig. 5

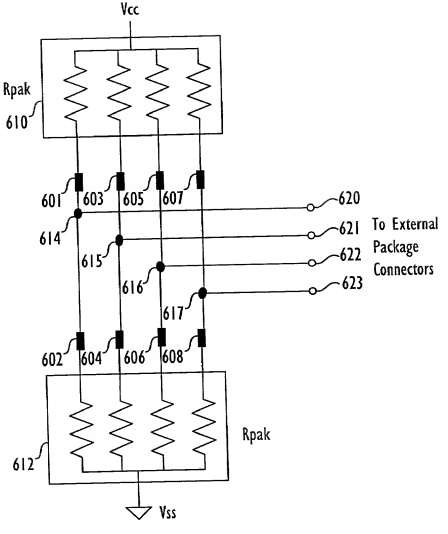
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Fig. 6

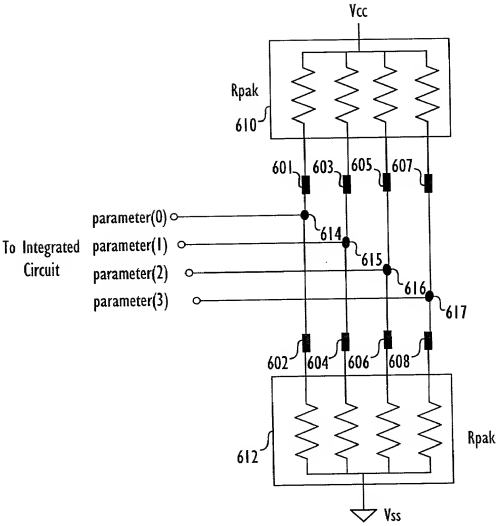

Fig. 7

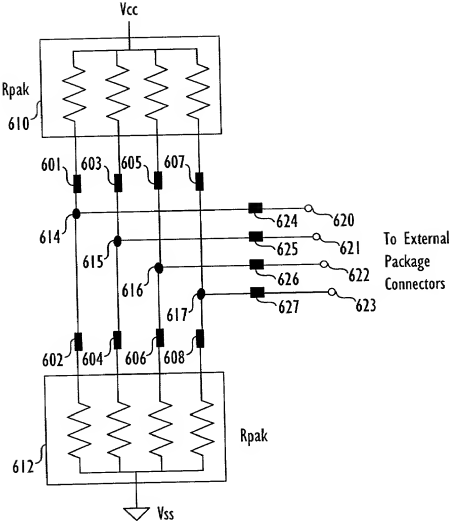
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Fig. 8

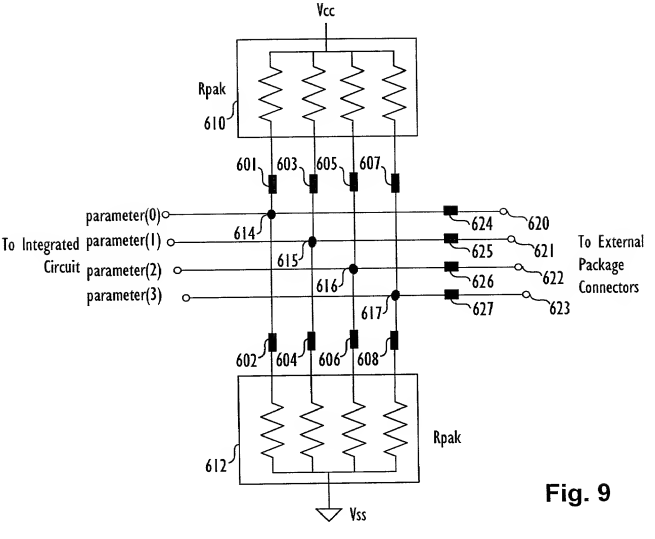

Fig. 9

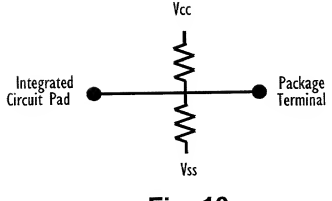

Fig. 10

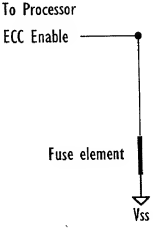

Fig. 11

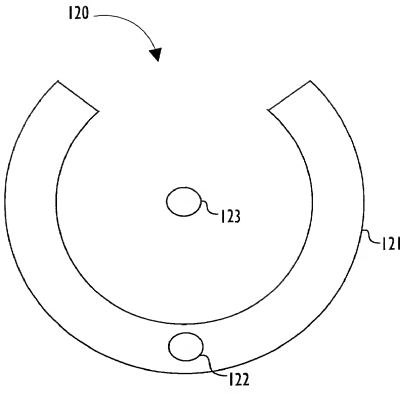

Fig. 12

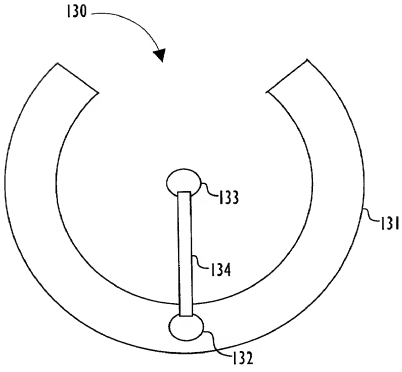

Fig. 13

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

INTEGRATED CIRCUIT PACKAGE INCORORATING PROGRAMMABLE ELEMENTS

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A				

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith:

Mark Zagorin (36,067); Andrew C. Graham (36,531); David W. O'Brien (40,107); Margaret M. Kelton (44,182); Paul S. Drake (33,491); Vincenzo D. Pitruzzela (28,656); Louis A. Riley (39,817); William D. Zahrt, II (26,070); Richard J. Roddy (27,688); and Elizabeth A. Apperley (36,428).

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the individual and/or firm named below:

Customer Number 22120
ZAGORIN, O'BRIEN & GRAHAM, L.L.P.
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AUSTIN, TX 78746

Telephone: (512) 347-9030
Facsimile: (512) 347-9031

USPTO Customer Number
022120
PATENT AND TRADEMARK OFFICE

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole (or first joint) inventor: James John Casto

Inventor's Signature: James John Casto Date: 13JAN2000
Residence: Lakeway, TX Citizenship: USA
Post Office Address: 1705 Idle Hour Cove
Lakeway, TX 78734

Full name of second joint inventor: Qadeer Ahmad Qureshi

Inventor's Signature: _____ Date: _____
Residence: Round Rock, TX Citizenship: USA
Post Office Address: 16708 Tomcat Drive
Round Rock, TX 78681

Full name of third joint inventor: Hugh William Boothby

Inventor's Signature: Hugh W. Boothby Date: 14 JAN 2000
Residence: Austin, TX Citizenship: USA
Post Office Address: 8823 North Madrone Trail
Austin, TX 78737

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

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Prior Foreign Application(s)			Priority Claimed	
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Inventor's Signature: _____ Date: 1/14/00
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